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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/334,238	06/16/1999	MICHAEL L. LONGWELL	JMS009-00	5116

7590 02/09/2006

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EXAMINER	
TU, CHRISTINE TRINH LE	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/334,238	LONGWELL ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-9 and 11-15 and 17-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-9,11-15 and 17-23* is/are allowed.

6)☒ Claim(s) *24-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-5 and 10 have been cancelled.

2. Claims 6-9, 11-37 have been examined.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

4. Claims 24-30 and 36 and 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24:

At line 12, it is not clear where is "a respective bit to be stored" coming from? And where is "a respective bit to be stored" going to be stored?

At line 13, it is not clear which bit the term "the corresponding stored bit" referring to? Where exactly is "the corresponding stored bit" is being stored?

At lines 12-13, the phrase "each parity bit is changed only if a bit to be stored is different from the corresponding stored bit" cannot be understood. It is not clear how each parity bit can be changed because each of n parity bits is generated and each parity bit is related to all m bits stored in respective one of the said column (as being recited at lines 9-11).

In other words, it is not clear whether each of n parity bits is generated/changed based on "all m bits stored in respective one of said columns" (as being recited at line 11), or based on the condition "if a respective bit to be stored is different from the corresponding stored bit" (as being recited at lines 12-13).

Claim 27:

At line 14, it is not clear where is "a respective bit to be stored" coming from? And where is "a respective bit to be stored" going to be stored?

At lines 1-15, it is not clear which bit the term "the corresponding stored bit" referring to? Where exactly is "the corresponding stored bit" is being stored?

At lines 13-15, the phrase "each check bit is changed only if a bit to be stored is different from the corresponding stored bit" cannot be understood. It is not clear how each check bit can be changed because each of a plurality of check bits is generated and each check bit is related to a unique combination of at least two of said bits stored in a respective one of said column (as being recited at lines 10-13).

In other words, it is not clear whether each of a plurality of check bits is generated/changed based on "a unique combination of at least two of said bits stored in a respective on of said columns" (as being recited at lines 12-13), or based on the condition "if a respective bit to be stored is different from the corresponding stored bit" (as being recited at lines 14-15).

Claims 25-26, 28-30 and 36-37:

These claims are rejected because they depend on claims 24 and 27 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 102

5. Claims 24-25, 27-28 and 31-35 are rejected under 35 U.S.C. 102(e) as being anticipated by McGinn (6,216,251).

Claims 24-25, 27-28 and 31-35:

The rationale for rejecting these claims is again the same as it was set forth in paragraph 5 of the previous office action which was mailed on August 1, 2005.

Claim Rejections - 35 USC § 103

6. Claims 26, 29-30 and 36–37 are rejected under 35 U.S.C. 103(a) as being unpatentable over McGinn (6,216,251).

Claims 26 and 29-30:

The rationale for rejecting these claims is again the same as it was set forth in paragraph 8 of the previous office action which was mailed on August 1, 2005.

Claims 36 and 37:

McGinn does not explicitly teach that the bit stored in each cell is initialized t a selected value prior to operation of the circuit. However, McGinn teaches that in a parity generation operation, a parity controller (208) first generates a parity bit for the data stored in each column of memory array (200) (column 3 lines 46-51). It would have been obvious to one skilled in the art at the time the invention was made to realize that the data is being initialized in each column of the memory array (200) prior to McGinn's parity generation operation. One having ordinary skill in the art would be motivated to realize that McGinn's data in each column of the memory array (200) would have been initialized or stored in advance in order to McGinn's parity controller to generate the parity based on such data initialized/stored in each column of the memory array (200).

Response to Arguments

7. Applicant's arguments filed November 04, 2005 have been fully considered but they are not persuasive.

For claims 24-25, 27-28, Applicant states that McGinn does not disclose applicant's system having a write operation to a selected address requires reading of only the signal word stored at the selected address, comparison of the "old" stored word to the "new" word to be stored and then updating the parity bits based on the results of that comparison. However, these limitations are not explicitly recited in the claims.

Firstly, NO comparing feature is being recited in the claims. Secondly, NO updating feature for any parity bit is being recited in the claims. What is being recited is generating feature (in the parity/code generating circuit) for generating n parity bits/a plurality of check bits and each (of the check bits/parity bits) related to bits being stored in respective on of said columns.

In addition, as being rejected by 112/2nd above (see paragraph 4 above for claims 24 and 27), it is not clear where is "a respective bit to be stored" coming from, and where is "a respective bit to be stored" going to be stored. It is also not clear which bit the term "the corresponding stored bit" referring to, and where exactly is "the corresponding stored bit" is being stored.

For claims 31-35, applicant argues that nothing in McGinn suggests that the method (or circuits) disclosed therein is applicable to an "ordered string" and in particular to an "ordered string" received "in any order". However, Examiner respectfully traverses applicant's remark. Firstly, McGinn's data (being stored in N column by M row memory array (200) [figure 2, column 2 lines 61-62 and column 3 lines 47-48]) is equivalent to the recited "ordered string". Secondly, applicant should aware that 'received (data/bits) "in any order"' is being recited. In other words, the claims are not recited with any specific/particular way to receive data/bits. Thus, "received (data/bits) "in any order"' can surely be data from each column of the memory array (as taught by McGinn—column 3 lines 47-48).

Applicant further argues that McGinn does not teach the parity generation circuit for generating plurality of parity bits, each (parity bit) related to a unique combination of said bits. Such limitation surely is taught by McGinn. McGinn teaches that the parity controller (208) generates a parity bit for the data stored in **each** column of memory array and stores these **(parity) bits (plural)** into memory array (200) (column 3 lines 46-49) [note: McGinn's array (200) has N columns (column 2 lines 61-62), therefore N parity bit**s** (plural) would be generated]. In other words, McGinn first explains how each parity bit is generated and then eventually (plurality of) N parity bit**s** are generated due to N columns in the memory array (200).

Furthermore, the limitation of "each (parity bit) related to a unique combination of said bits comprising said string" can be McGinn's a parity for the data stored in each column of memory array (200). This is because the recitation of "unique combination of said bits" is not excluded from the inclusion of data (bits) in a (or each) column of McGinn's memory array (200).

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2138

February 3, 2006